# ESD Protection Design for 900-MHz RF Receiver with 8-kV HBM ESD Robustness

Ming-Dou Ker, Wen-Yu Lo, Chien-Ming Lee, Chia-Pei Chen*, and Hong-Sing Kao*

Integrated Circuits & Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan

*R&D Division
Alfaplus Semiconductor Inc.
Science-Based Industrial Park, Hsinchu, Taiwan

***Abstract* – *This paper presents a state-of-art ESD protection design for RF circuit with a human-body-model (HBM) ESD robustness of 8kV. By including a turn-on efficient power-rails clamp circuit into the RF circuit, the ESD clamp devices of the RF input pin are operated in the forward-biased conduction, rather than the traditional junction breakdown condition. Therefore, the dimension of ESD devices for the RF input pin can be further downsized to reduce the input capacitance loading for the RF signal. This design has been successfully applied in a 900-MHz RF receiver and fabricated in 0.25-μm CMOS process with a thick top metal layer. The experimental results have confirmed that its ESD robustness is as high as >8kV under the HBM ESD test.***

## I. INTRODUCTION

Due to the low breakdown voltage of the much thinner gate oxide in sub-quarter-micron CMOS technologies, the effective on-chip electrostatic discharge (ESD) protection circuit should be designed and placed on every input / output pad to clamp the overstress ESD voltage. The traditional ESD protection design with the two-stage protection structure for digital IC's is shown in Fig.1. Between the primary stage and the secondary stage of the input ESD protection circuit, a resistor is added to limit the ESD current flowing through the short-channel NMOS in the secondary stage. The resistance value of this resistor is dependent on the turn-on voltage of the ESD clamp device in the primary stage and the It2 (secondary breakdown current) of the short-channel NMOS in the secondary stage. Such two-stage ESD protection design can provide high ESD level for the digital input pins. But the large series resistance and the large junction capacitance in the ESD clamp devices cause a long *RC* timing delay to the input signal, it is no longer suitable for analog pins, especially for the RF signal applications.

For RF front-end circuits [1]-[4], input ESD protection circuit has limitations on the loading capacitance and the noise figure. A typical request for an RF input pad with maximum loading capacitance is only 200 fF for circuit operation at 2 GHz [5]. The diodes with smaller parasitic capacitance (as compared to the gate-ground NMOS) are commonly used for ESD protection in RF circuits [2], [3], [6]. However, the actually measured data from the practically fabricated LNA chips with on-chip ESD protection designs [2], [3] have shown that the ESD robustness was only around 1~2kV. With such an ESD level, it is still too low for safe production during the IC assembly and testing.

To further improve impedance matching for RF signal, the ESD protection devices were even separated into multiple sections [7], [8]. But, it is hard to achieve uniform ESD current distribution among the multiple separated ESD sections during the fast ESD events. The first ESD section, which closes to the input pad, is often damaged by ESD, before the second or third sections are turned on to share ESD current. Therefore, it could cause a low ESD level in the practical chip, even if it has multiple ESD protection sections. So, on-chip ESD protection design is still a challenge to RF front-end circuits, especially for the RF receiver with LNA.

In this paper, a state-of-art ESD protection design with 8-kV HBM ESD robustness for RF circuits is first reported in the literature. This ESD protection design has been practically used in a 900-MHz RF receiver IC, which is fabricated in 0.25-μm CMOS process with a thick top metal layer.

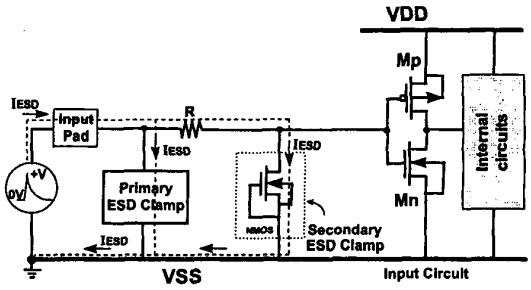


Fig.1 The traditional two-stage ESD protection circuit for digital input pin in CMOS IC's.

## II. ESD PROTECTION DESIGN FOR RF RECEIVER

To investigate the ESD robustness of input / output pins in IC's, the pin combinations during the ESD stress had been specified in the standard [9]. For an input pin, there are four basic ESD-stress modes, as shown in Fig.2, where the positive or negative ESD voltage is applied to



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an input pin with the VDD or VSS pins relatively grounded. The ESD level of the tested pin is defined as the lowest ESD level among the four-modes ESD stresses. Therefore, the on-chip ESD protection design should provide effective discharging paths for these four-modes ESD stresses.

The proposed ESD protection design for the 900-MHz RF receiver is shown in Fig.3. In order to reduce the loading capacitance to the LNA RF input pin, the diodes are designed with a small device dimension. With a small device dimension, the NDIO (PDIO) diode under the PS-mode (ND-mode) ESD stress operated in the junction breakdown to discharge ESD current often has a low ESD level. To avoid the small diodes (NDIO and PDIO in Fig.3) operated in the breakdown condition during the PS-mode and ND-mode ESD stresses to cause a much low ESD level, a turn-on efficient ESD clamp circuit between the power rails is constructed into the ESD protection circuit to significantly increase the overall ESD level. The turn-on efficient power-rail ESD clamp circuit is shown in Fig.4 [10]. The overall circuit block of the 900-MHz RF receiver with the ESD protection design is shown in Fig.5. The 900-MHz output signal of LNA is down converted to 10.8-MHz signal by the following mixer.

When the RF_input pin is zapped in the NS-mode (PD-mode) ESD stress, the NDIO (PDIO) diode is operated under the forward-biased condition to discharge ESD current. The diode operated under the forward-biased condition can sustain a much higher ESD level than it operated in the reverse-biased breakdown condition. In Fig.4, the *RC*-based ESD detection circuit is used to trigger on the MNESD device, when the RF_input pad is zapped with the PS-mode or ND-mode ESD stresses. The ESD current paths in this RF ESD protection design under the PS-mode and ND-mode ESD stresses are illustrated by the dashed lines in Figs. 6(a) and 6(b), respectively. Because the NDIO diode in the PS-mode ESD stress is not operated in the breakdown condition, the ESD current is bypassed through the forward-biased PDIO diode and the turned-on MNESD between the VDD/VSS power rails. Similarly, the ND-mode ESD current is discharged as the dashed line shown in Fig.6(b) with the NDIO diode operated in the forward-biased condition and the turned-on MNESD between the VDD/VSS power rails. The MNESD is especially designed with a larger device dimension (960/0.5) to sustain a high ESD level. Although the large-dimension MNESD has a large junction capacitance, this capacitance does not contribute to the RF_input pad. By using the proposed ESD protection design, the RF_input pin can sustain much higher ESD levels in the four-mode ESD stresses but only with small diodes connected to the RF_input pad. Therefore, the loading capacitance generated from the ESD protection devices to the RF_input pad can be significantly reduced.

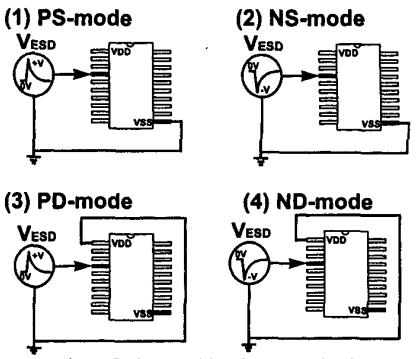



Fig.2 Four modes of pin combinations on the input or output pin of an IC under the Human-Body-Model (HBM) ESD test.

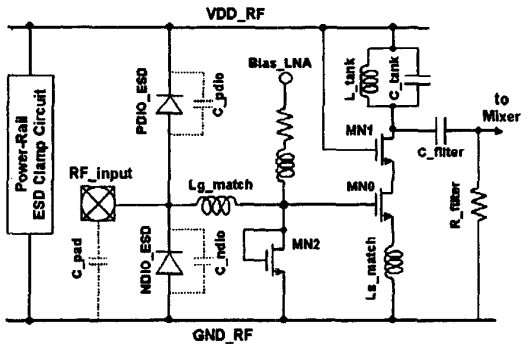



Fig.3 The proposed ESD protection circuit for LNA RF input pin.

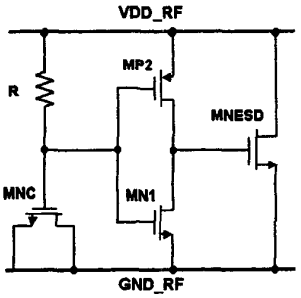



Fig.4 The detailed design of the turn-on efficient power-rail ESD clamp circuit for the LNA RF circuit.

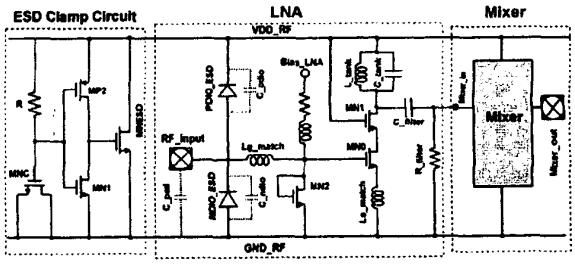
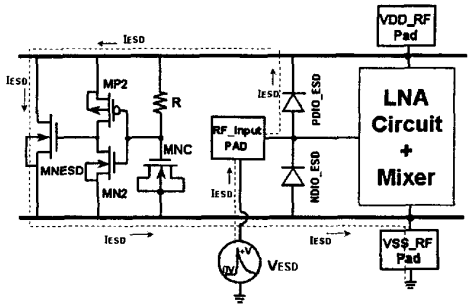
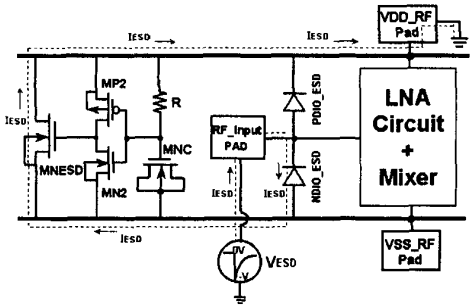



Fig.5 The overall circuit block of the 900-MHz RF receiver.




(a)




(b)

Fig.6 The ESD current path along the proposed RF ESD protection circuit when the input pin is tested in (a) the PS-mode, (b) the ND-mode, ESD stress.

To further reduce the parasitic capacitance at the RF input node, the RF_input pad is realized by only metal3, metal4, and metal5 in a 0.25-μm CMOS process of 5 metal layers. The shape of the bond pad is a square with a layout area of $75x75\mu m^2$. There is also an N-well with a square shape and a layout area of $80x80\mu m^2$ laid beneath the bond pad for reducing the parasitic capacitance between the bond pad and the P-substrate.

## III. Experimental Results

This 900-MHz RF receiver with on-chip ESD protection design has been practically fabricated in a 0.25-μm CMOS process with a thick top metal layer for inductor application. The actual device dimension used in the on-chip ESD protection circuit is summarized in Table I. Each finger of NDIO and PDIO diodes has a layout area of only $3x30\ \mu m^2$. Three fingers are placed in parallel from the pad to VDD_RF (VSS_RF) for the NDIO (PDIO) diodes. The metal option can be used to adjust the number of diode fingers connected to RF_input pad for different loading capacitance specifications. The resistor R is realized by the N-well resistance, which has a sheet resistance of 1100 ohm/sq. The gate oxide of NMOS MNC has a Cox of $4.9fF/\mu m^2$.

### *A. ESD Test Results*

The HBM (human-body model) and MM (machine model) ESD test results on the fabricated 900-MHz RF receiver IC are summarized in Table II, which includes the four-modes ESD stresses and the VDD-to-VSS ESD stress. As shown in Table II, the proposed ESD protection circuit can successfully provide the RF_input pin with an HBM (MM) ESD level of greater than 8000V (900V) in each ESD-stress condition. The failure criterion is defined as the leakage current greater than 1μA under 3.3V bias. After the 8000-V HBM ESD stress, the leakage current from the RF_input pin to VDD and VSS is still around 8~15nA, which is almost the same as the original leakage current of the RF_input pin before ESD zapping. To double verify the ESD robustness of the proposed ESD protection design, the TLP (transmission line pulse) is used to measure the It2 (second breakdown current) of the ESD protection circuit. The TLP-measured I-V curve of the RF_input pin under the PS-mode ESD stress condition is shown in Fig.7, where it has an It2 as high as ~6.5A which is corresponding to a HBM ESD level of ~9.7kV. This has verified the effectiveness of the proposed on-chip ESD protection circuit for the 900-MHz RF receiver.

Table I Layout sizes of the ESD protection circuit.

| | Width (μm) | Length (μm) | Unit Width (μm) | Multiple |
|---|---|---|---|---|
| MNESD | 960 | 0.5 | 30 | M=32 |
| MN1 | 180 | 0.35 | 15 | M=12 |
| MP2 | 240 | 0.30 | 15 | M=16 |
| MNC | 45 | 13 | 15 | M=3 |
| PDIO_ESD | 2 | 30 | | M=3 |
| NDIO_ESD | 2 | 30 | | M=3 |
| R | 3 | 130.5 | | |

Table II ESD Test Results

| | Pin Combination in ESD Test | | | | |
|---|---|---|---|---|---|
| | PS-mode | NS-mode | PD-mode | ND-mode | VDD-to-VSS |
| HBM (V) | > 8000 | > 8000 | > 8000 | > 8000 | > 8000 |
| MM (V) | > 900 | > 900 | > 900 | > 900 | > 900 |

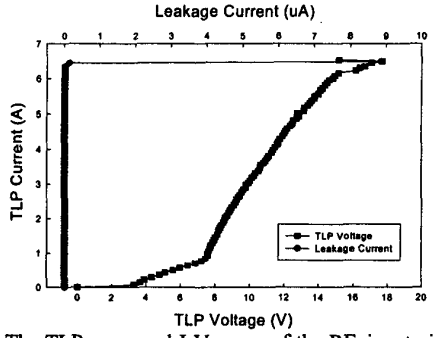



Fig.7 The TLP-measured I-V curve of the RF_input pin under the PS-mode ESD stress condition.

*B. RF Performance*

The power gain of the fabricated 900-MHz RF receiver with or without the ESD protection circuit has been measured and compared in Fig.8. The RF receiver with the ESD device has a maximum power gain of 14.8dB at the frequency of 920MHz. The RF receiver without any ESD device has a maximum power gain of 15.8dB at the frequency of 930MHz. The proposed on-chip ESD protection circuit only causes a 10-MHz shifting in frequency and 1-dB shifting in power gain on the 900-MHz RF receiver. The measured power gain of the fabricated 900-MHz RF receiver with ESD device is still good enough for circuit applications.

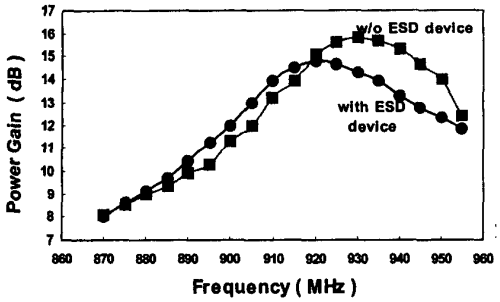
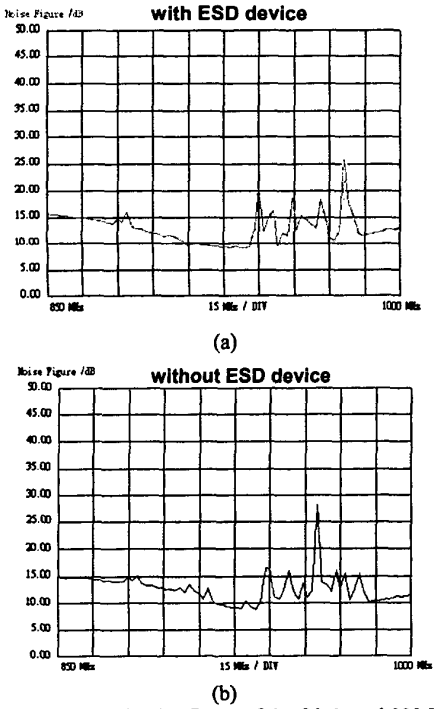



Fig.8 The measured power gain of the fabricated 900-MHz RF receiver with or without the ESD protection circuit.




(a)

(b)

Fig.9 The measured noise figure of the fabricated 900-MHz RF receiver (a) with, and (b) without, the ESD protection circuit.

The noise figure of the fabricated 900-MHz RF receiver with or without the ESD device has been also measured and compared in Figs. 9(a) and 9(b), respectively. At the application frequency range around 910~920 MHz, the noise figure of the RF receiver (including LNA and mixer) in Figs. 9(a) and 9(b) is around 8~10dB. The on-chip ESD protection circuit does not cause any obvious increase on the noise figure of the overall RF receiver. This has confirmed that the RF receiver with the proposed on-chip ESD protection circuit still has good enough RF performance.

## VI. CONCLUSION

An on-chip ESD protection design with low enough input capacitance and high enough ESD level has been actually verified with a 900-MHz RF receiver in a 0.25-μm CMOS process. The HBM ESD level of the LNA RF_input pin of the 900-MHz RF receiver has been successfully improved up to >8kV. The RF performance of power gain and noise figure is still good enough for the 900-MHz RF receiver protected by the proposed on-chip ESD protection design.

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